microSD/
microSDHC

Datasheet

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Revision History

Revision	Date	History	Remark
A.0	12/12 '07	New Creation	

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1. Introduction to the microSD/SDHC

microSD Card is a Flash – Based memory card that is designed to meet the security, capacity, performance and environment requirements inherent to use in emerging audio and video electronic device.
The microSD Card communication is based on an advance 8-pin interface (clock, command, 4x Data and 2x power lines) and the microSD Memory Card host interface supports regular MultiMediaCard operation as well.

2. microSD/SDHC Feature

- Flash memory card capacity support list below:
  - 128MB
  - 256MB
  - 512MB
  - 1GB
  - 2GB

  High capacity microSDHC support list below:
  - 4GB
  - 8GB
  - 16GB
  - 32GB

  Only hosts that are compliant o the Physical Layer Specification version2.00 or higher and the SD File system specification ver2.00 can access High Capacity SD Memory Cards.
  Other hosts fail to initialize High Capacity miroSDHC .(See Figure 2-1)

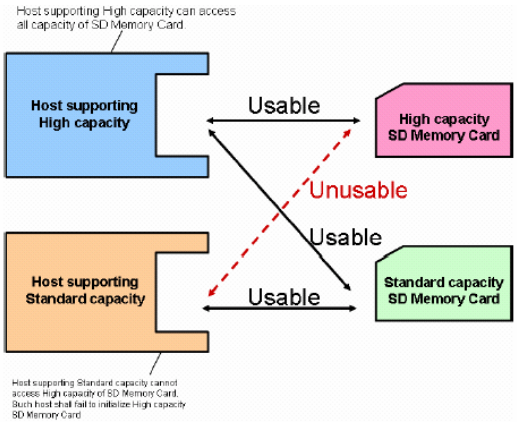


Figure 2-1 Host-Cards Usability

- Compliant SD Card Specification ver 2.0
- Variable clock rate:
  - Default mode: 0-25 MHz, up to 12.5MB/sec interface speed.
  - High-speed mode:0-50 MHz, up to 25MB/sec interface speed.

- High Capacity microSDHC shall support Speed Class Specification and have performance more Than or equal to Class 2, it includes:
  - Class 2 – Are more than or equal to 2MB/sec performance.
  - Class 4 – Are more than or equal to 4MB/sec performance.
  - Class 6 – Are more than or equal to 6MB/sec performance.

- Dimension: 15.0mm x 11.0mm
- Support CPRM
- No external programming voltage required
- SD Memory Card protocol compatible
- Targeted for portable and stationary applications for secured (copyrights protected) and non-secured data storage
- Correction of memory field errors
- Copyrights Protection Mechanism: Complies with highest security of SDMI standard
- Card Detection (Insertion / Removal)
- CE and FCC certificates
- Easy handling for the end user

Notes: The performance depends on different test platform with different result.

- The communication channel is described in the table below

microSD/SDHC Bus/SPI Bus comparison

microSD/SDHC Using SD Bus	microSD/SDHC Using SPI Bus
Six-wire communication channel (clock, command, 4 data lines)	Three-wire serial data bus (Clock, dataIn, dataOut)+card specific CS signal(hardwired card selection)
Error-protected data transfer	Optional non protected data transfer mode available
Single or multiple block oriented data transfer	Single or multiple block oriented data transfer

3. Product Specification

3.1 Reliability and Durability Specifications

Temperature	Operating: -25℃ to 85℃ Storage: -40℃(168h) to 85℃(500h)
moisture and corrosion	Operating: 25℃ / 95% rel. humidity Non-Operating: 40℃ / 93% rel. hum./500h salt water spray: 3% NaCl/35C; 24h acc. MIL STD Method 1009
Durability	10,000 mating cycles
Bending	10N
Torque	0.10N*m. ±2.5° max
Drop Test	1.5m free fall
UV Light Exposure	UV: 254nm, 15Ws/cm^2 according to IOS 7816-1
Visual Inspection/Shape and Form	No warp age; no mold slim; complete form; no cavities; surface smoothness≦-0.1 mm/ cm^2 within contour; no cracks; no pollution (oil, dust, etc.)

3.2 System Reliability and Maintenance

MTBF	>1,000,000 hours
Preventive Maintenance	None
Data Reliability	< 1 non-recoverable error in 10^{14} bits read
Endurance	300,000 write/erase cycles

3.3 Electrical Static Discharge (ESD) requirement

ESD Protection	Contact Discharge: Air Discharge;	±4KV, Human body model according to IEC61000-4-2.EN55024 ±8KV, Human body model according to IEC61000-4-2.EN55024

4. microSD/SDHC Interface Description

4.1 General Description of Pins and Registers

The microSDHC has nine exposed contacts on one side. The host is connected to the SD Memory Card using a eight pin connector.

Pin Assignment in SD Bus Mode Pad Definition

Pin #	Name	Type	microSD Description
1	DAT2	I/O	Card Detect/ Data Lin [Bit 3]
2	CD/DAT3	I/O	Card Detect / Data Line
3	CMD	PP	Command / Response
4	VDD	S	Supply voltage
5	CLK	I	Clock
6	Vss	S	Supply voltage ground
7	DAT0	I/O	Data Line [Bit 0]
8	DAT1	I/O	Data Line [Bit 1]

Note:

1) S=power supply; I=input; O=output using push-pull drivers.

2) The extended DAT lines (DAT1-DAT3) are input on power up; they start to operate as DAT lines after the SET_BUS_WIDTH command.

3) After power up, this line is input with 50Kohm pull-up (can be used for card detection or SPI mode selection). The pull-up should be disconnected by the user, during regular data transfer, with SET_CLR_CARD_DETECT (ACMD42) command.

Pin Assignment in SPI Bus Mode Pad Definition

Pin #	Name	Type	microSD Description
1	RSV		Reserved
2	CS	I	Chip Select (neg true)
3	DI	S	Data In
4	VDD	S	Supply Voltage
5	SCLK	I	Clock
6	VSS	S	Supply Voltage Ground
7	DO	O	Data Out
8	RSV	I	Reserved

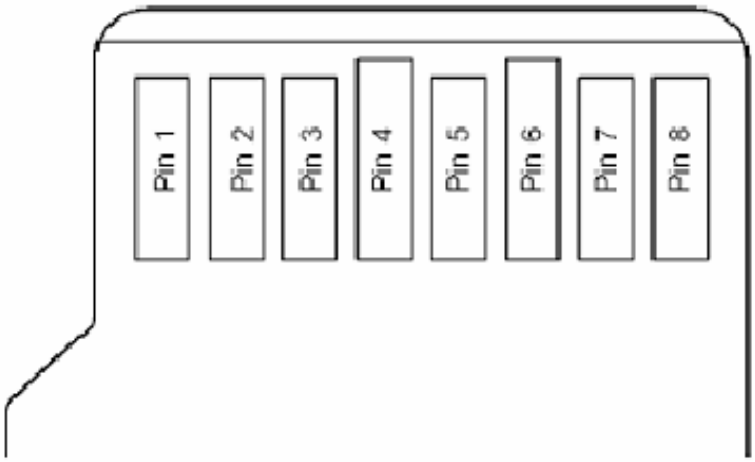
Each card has a set of information registers

microSD Memory Card Registers

Name	Width	Description
CID	128	Card identification number: individual card number for identification.
RCA	16	Relative card address: local system address of a card dynamically suggested by the card and approved by the host during initialization
CSD	128	Card specific data: information about the card operation conditions.
SCR	64	SD Configuration Register: information about the microSD Card's special feature capabilities.
OCR	32	Operation Condition Register

The host may reset the cards by switching the power supply off and on again. The card has its own power-on detection circuitry which puts the card into an idle state after the power-on. The card can also be reset by sending the GO_IDLE (CMD0) command.

microSD memory Card Pin Assignment



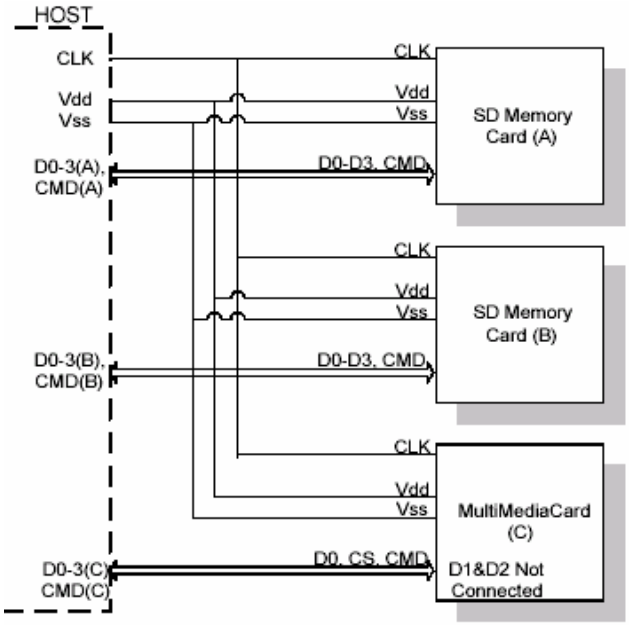
microSD memory Card contact Area

4.2 SD Bus Topology

The SD bus has six communication lines and three supply lines:

- CMD: Command is bi-directional signal.(Host and card drivers are operating in push pull mode.)
- DAT0-3: Data lines are bi-directional signals. (Host and card drivers are operating in push pull mode.).
- CLK: Clock is a host to cards signal. (CLK operates in push pull mode.)
- VDD: VDD is the power supply line for all cards.
- VSS [1:2]: VSS are two ground lines.
-

The following figure shows the bus topology of several cards with one host in SD Bus mode.



microSD Memory Card System Bus Topology

During the initialization process, commands are sent to each card individually, allowing the application to detect the cards and assign logical addresses to the physical slots. Data is always sent to each card individually. However, to simplify the handling of the card stack, after initialization, all commands may be sent concurrently to all cards. Addressing information is provided in the command packet.
The microSD Bus allows dynamic configuration of the number of data lines. After power-up, by default, the microSD Memory Card will use only DAT0 for data transfer. After initialization, the host can change the bus width (number of active data lines). This feature allows and easy trade off between hardware cost and system performance.

4.2.1 Power Protection
Card can be inserted into or removed from the bus without damage. If one of the supply pins (VDD or Vss) is not connected properly, then the current is drawn through a data line to supply the card.
Data transfer operations are protected by CRC codes; therefore, any bit changes induced by card insertion and removal can be detected by the microSD bus master. The inserted card must be properly reset also when CLK carries a clock frequency f_{pp}.
If the hot insertion feature is implemented in the host, than the host has to withstand a shortcut between VDD and Vss without damage.

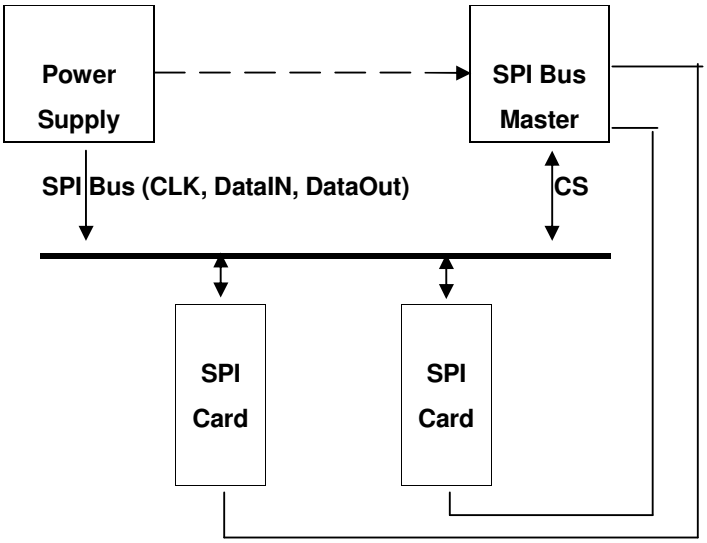
4.3 SPI Bus Topology
The memory Card SPI interface is compatible with SPI hosts available on the market. As any other SPI device the microSD Memory Card SPI channel consists of the following 4 signals:

1) CS: Host to card Chip Select signal.
2) SCLK: Host to card clock signal.
3) DataIn: Host to card data signal.
4) DataOut: Card to host data signal.

Another SPI common characteristic, which is implemented in the Memory Card as well, is byte transfers. All data tokens are multiples of 8 bit bytes and always byte aligned to the CS signal.

The SPI standard defines the physical link only and not the complete data transfer protocol. In SPI Bus mode, the microSD Memory Card uses a subset of the microSD Memory Card protocol and command set.
The microSD Memory Card identification and addressing algorithms are replaced by a hardware Chip Select (CS) signal. A card (slave) is selected, for every command, by asserting (active low) the CS signal.
The CS signal must be continuously active for the duration of the SPI transaction (command, response and data). The only exception is card programming time. At this time the host can de-assert the CS signal without affecting the programming process.

The bi-directional CMD and DAT lines are replaced by uni-directional dataIn and dataOut signals. This eliminates the ability of executing commands while data is being read or written. An exception is the multi read/write operations. The Stop Transmission command can be sent during data read. In the multi block write operation a Stop Transmission token is sent as the first byte of the data block.



SD Memory Card Bus System

4.4 Electrical Interface

The power up of the SD Memory Card bus is handled locally in each SD Memory Card and in the bus master.

4.4.1 Operating Conditions

SPI Mode bus operating conditions are identical to SD Memory Card mode bus operating conditions. The CS (chip select) signal timing is identical to the input signal timing.

Power Supply Voltage

General					
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**	**Remark**
Peak voltage on all lines		-0.3	3.6	V	
All Inputs					
Input Leakage Current		-10	10	uA	
All Outputs					
Output Leakage Current		-10	10	uA	
Power supply Voltage					
Parameter	**Symbol**	**Min.**	**Max.**	**Unit**	**Remark**
Supply Voltage for High voltage range	V_{DDH}	2.7	3.6	V	
Supply voltage differentials (Vss1, Vss2)		-0.5	0.5	V	

Bus Signal Line Load

The total capacitance CL of the CLK line of the SD Memory Card bus is the sum of the bus master capacitance CHOST, the bus capacitance CBUS itself and the capacitance CCARD of each card connected to this line:

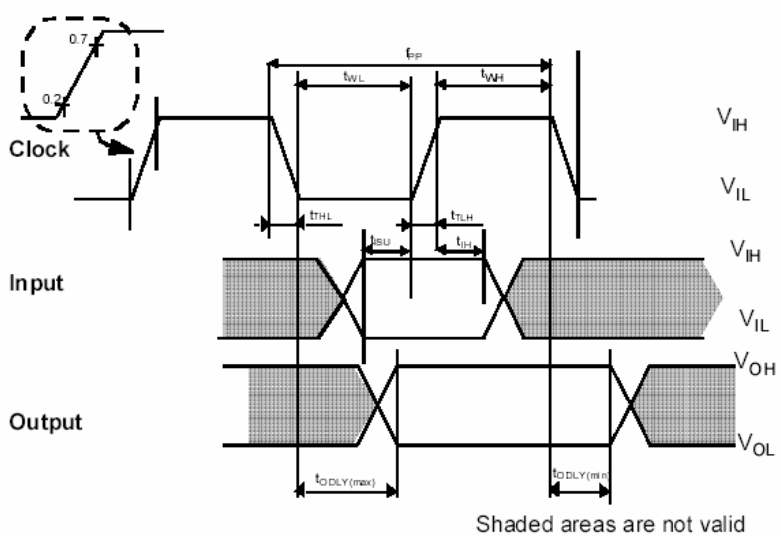
$$CL = CHOST + CBUS + N*CCARD$$

Where N is the number of connected cards. Requiring the sum of the host and bus capacitances not to exceed 30 pF for up to 10 cards, and 40 pF for up to 30 cards, the following values must not be exceeded:

Signal Line's Load

Parameter	Symbol	Min.	Max.	Unit	Remark
Pull-up resistance	R_{CMD}	10	100	kΩ	To prevent bus floating
Total Bus capacitance for each signal line	C_L		40	pF	Single Card C_{HOST} +C_{BUS} Shall not exceed 30 pF
Maximum signal line inductance			16	nH	fPP ≤ 20 MHz
Pull-up resistance inside card (pin1)	R_{DAT3}	10	90	kΩ	May be used for card detection

4.4.2 Bus Timing

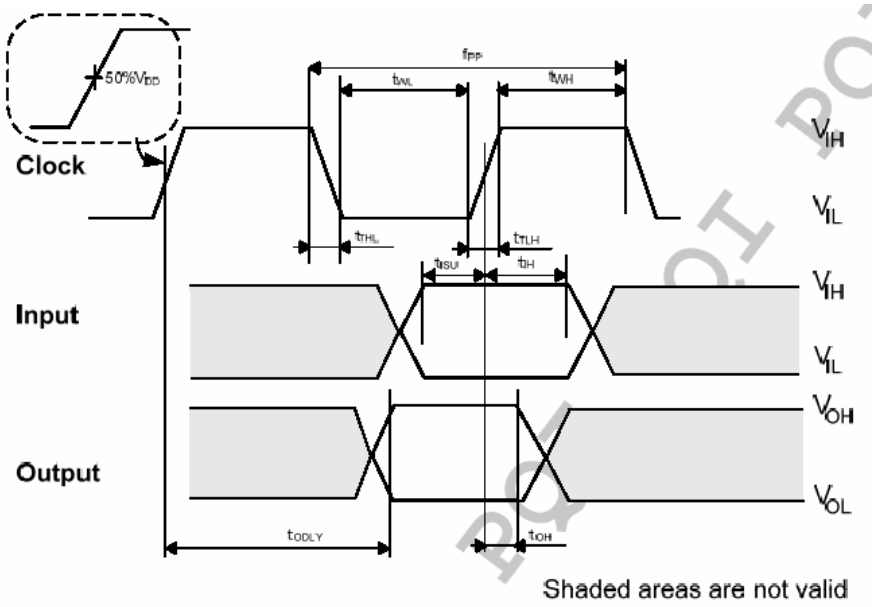


Timing Diagram Data Input. Output Referenced to Clock

Bus Timing (default mode)

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min.(VIH) and max.(VIL))					
Clock Frequency Data Transfer Mode	fPP	0	25	MHz	
Clock Frequency Identification Mode(The low frequency is required for SDCard compatibility)	fOD	0	400	KHz	
Clock Low Time	tWL	10		ns	
Clock High Time	tWH	10		ns	
Inputs CMD,DAT(referenced to CLK)					
Input set-up time	tISU	5		ns	
Input hold time	tIH	5		ns	
Outputs CMD,DAT(referenced to CLK)					
Output delay time during Data Transfer Mode	tODLY		14	ns	
Output delay time during Identification Mode	tODLY		50	ns	

4.4.3 Bus Timing (High-Speed Mode)



Bus Timing (High speed)

Parameter	Symbol	Min.	Max.	Unit	Remark
Clock CLK (All values are referred to min.(VIH) and max.(VIL))					
Clock Frequency Data Transfer Mode	fPP	0	50	MHz	
Clock Low Time	tWL	7		ns	
Clock High Time	tWH	7		ns	
Clock Rise Time	tTLH		3	ns	
Clock Fall Time	tTHL		3	ns	
Inputs CMD,DAT(referenced to CLK)					
Input set-up time	tISU	6		ns	
Input hold time	tIH	2		ns	
Outputs CMD,DAT(referenced to CLK)					
Output delay time during Data Transfer Mode	tODLY		14	ns	
Output Hold time	tODLY	2.5		ns	
Total System capacitance for each line	CL		40	pF	

4.5 microSD/SDHC Registers

There is a set of seven registers within the card interface. The OCR, CID, CSD and SCR registers carry the card configuration information. The RCA register holds the card relative communication address for the current session. The card status and SD status registers hold the communication protocol related status of the card.

4.5.1 Operating Conditions Register (OCR)

The 32-bit operation conditions register stores the VDD voltage profile of the card. The SD Memory Card is capable of executing the voltage recognition procedure (CMD1) with any standard SD Memory Card host using operating voltages form 2 to 3.6 Volts.
Accessing the data in the memory array, however, requires 2.7 to 3.6 Volts. The OCR shows the voltage range in which the card data can be accessed. The structure of the OCR register is described in under table.

OCR Register Definition

OCR Bit	VDD Voltage Window
0-3	Reserved
4	Reserved
5	Reserved
6	Reserved
7	Reserved
8	Reserved
9	Reserved
10	Reserved
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	2.7-2.8
16	2.8-2.9
17	2.9-3.0
18	3.0-3.1
19	3.1-3.2
20	3.2-3.3
21	3.3-3.4
22	3.4-3.5
23	3.5-3.6
24-29	Reserved
30	Card Capacity Status (CCS)
31	Card power up status bit (busy)

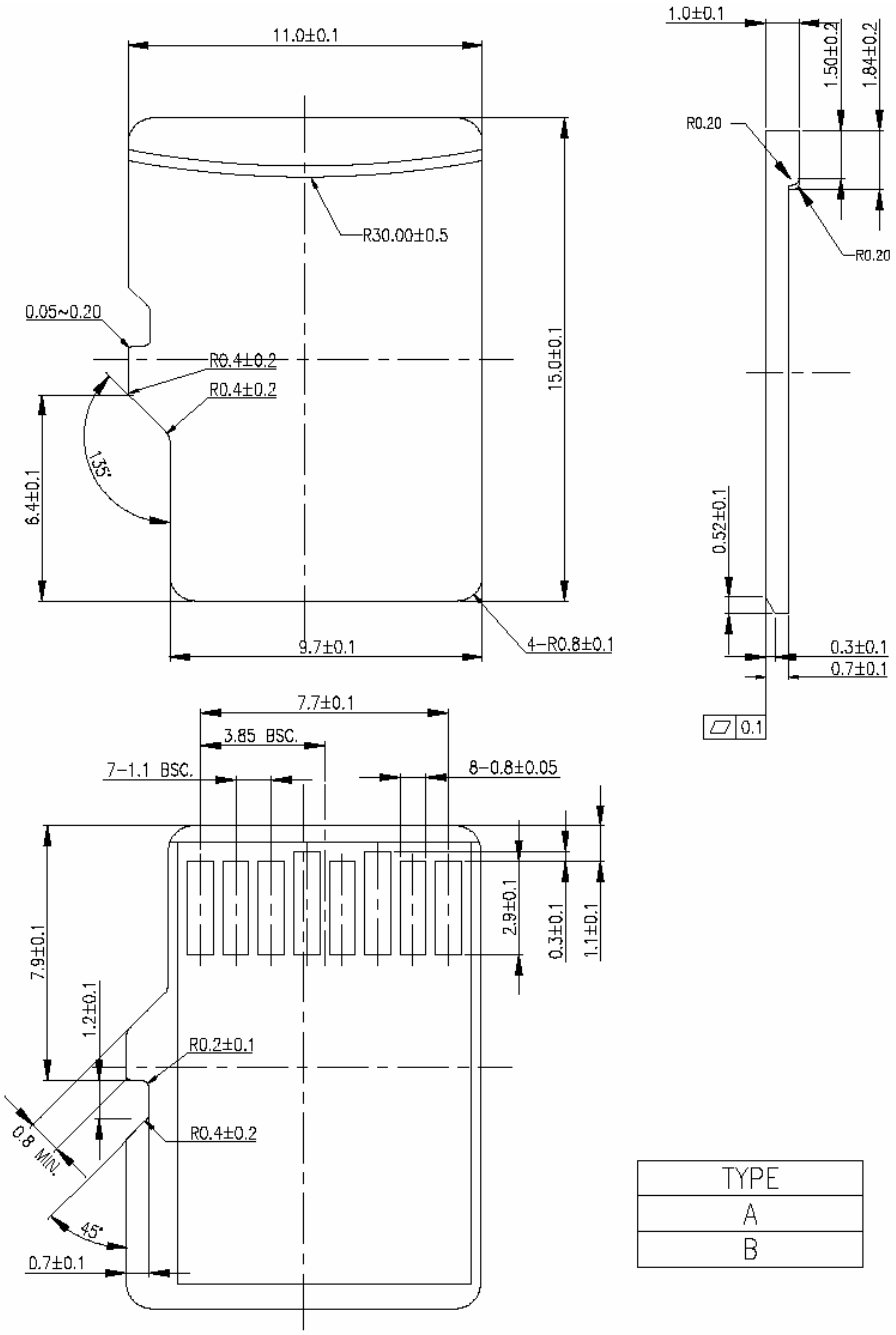
4.5.2 Card Identification (CID) Register

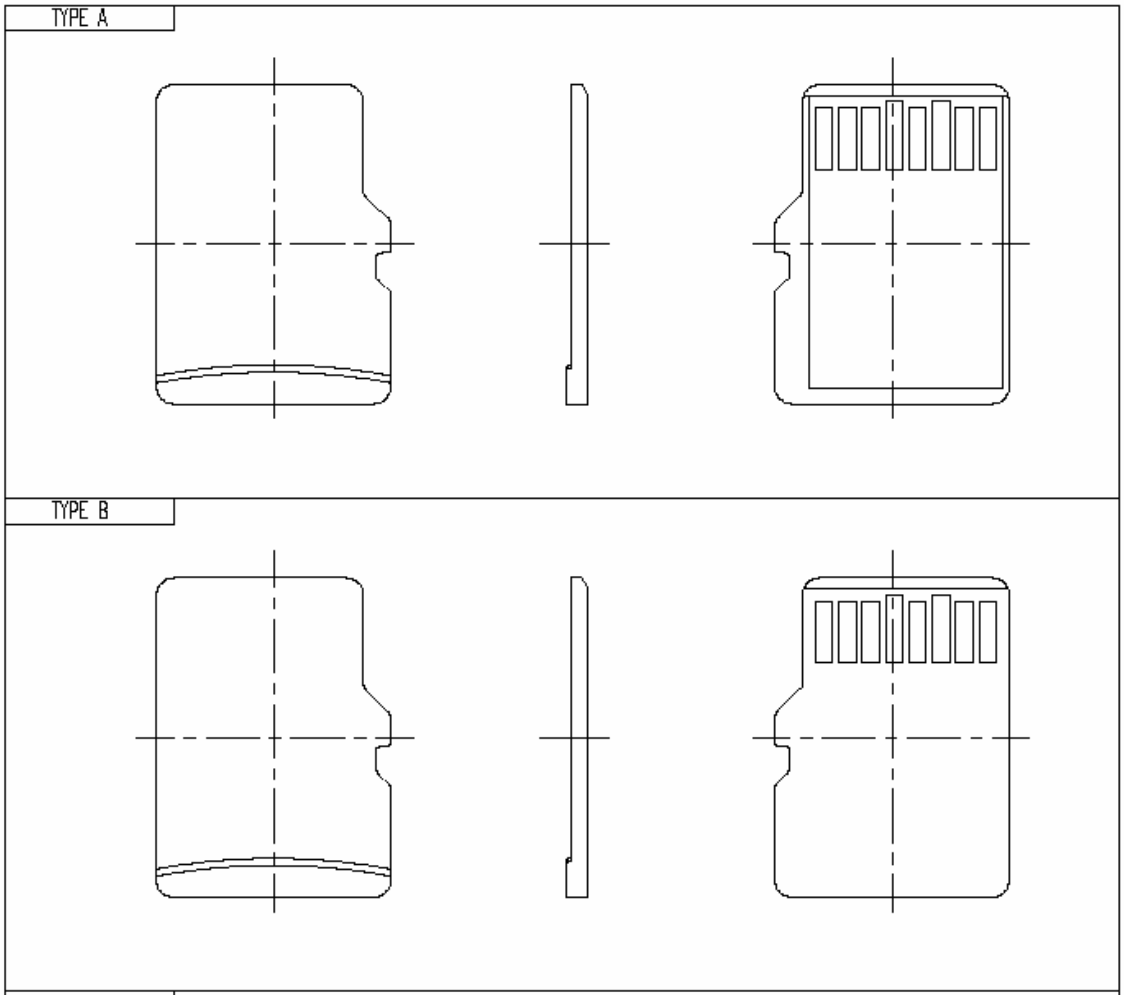
The CID register is 16 bytes long and contains a unique card identification number as shown in the table below. It is programmed during card manufacturing and can not be changed by SD Memory Card hosts. Note that the CID register in the SD Memory Card has a different structure than the CID register in the Multimedia Card

CID Fields

Name	Type	Width	CID - Slice	Comments
Manufacturer ID(MID)	Binary	8	[127:120]	The manufacturer IDs are controlled and assigned by the SD Memory Card Association.
OEM/Application ID(OID)	ASCⅡ	16	[119:104]	Identifies the card OEM and/or the card contents. The OID is assigned by the 3C.
Product Name(PNM)	ASCⅡ	40	[103:64]	5ASCⅡ characters long
Product Revision (PRV)	BCD	8	[63:56]	Two binary coded decimal digits
Serial Number (PSN)	Binary	32	[55:24]	32 Bits unsigned integer
Reserved		4	[23:20]	
Manufacturing Data Code(MDT)	BCD	12	[19:8]	Manufacturing date-yym(offset from 2000)
CRC7 checksum(CRC)	Binary	7	[7:1]	Calculated
Not used, always ‘1’		1	[0:0]	

5. Physical Outline




TYPE A
TYPE B